REMARKS/ARGUMENTS

Claims 16 and 18-20 are pending.

Claims 16-20 and 22-25 were rejected under 35 U.S.C. Section 112, 2nd paragraph. In response, claim 16 has been amended to cancel the term "critical." Claims 21-25 have been canceled without prejudice or disclaimer. The Section 112 rejection is believed to be overcome.

Claims 16-26 have been rejected under 35 U.S.C. Section 103 in view of Muckenhirn (U.S. Pat. Publ. No. 2003/0168594), Bendik et al. (U.S. Pat. No. 6,673,638), Demmin (U.S. Pat. No. 6,635,185), Singh et al. (U.S. Pat. No. 6,778,268), and Yoshitake et al. (U.S. Pat. Publ. No, 2003/0121022).

Claim 16, as amended, substantively recites in part performing "a preparation step" on a sample wafer to obtain first and second correspondence relationships between a test pattern and an actual circuit pattern formed on the sample wafer. Then, "an evaluation step" is performed on a manufactured wafer having its own test pattern and actual circuit pattern. An estimation of the actual circuit pattern of the manufactured wafer is then made based on the first and second correspondence relationships. See for example, the discussion of Figs. 11, 12A, and 12B in the specification.

As best understood, Muckenhirn is primarily related to integrating two instruments within a single instrument so that an optical instrument such as a scatterometer and a feature-measuring instrument such as a scanning probe microscope are integrated into the same tool. Muckenhirn teaches in Fig. 3 to form a test pattern on a production-line wafer. Muckenhirn does not show forming test patterns and actual circuit patterns on a sample wafer. Muckenhirm does not show obtaining first and second correspondence relationships between a test pattern and an actual circuit pattern formed on the sample wafer, and then using those correspondence relations to assess the production-line wafer.

Bendik teaches the formation of a test pattern for monitoring changes in exposure conditions and thereby process management. As best understood, the test structures appear to facilitate correct focusing on the wafer by virtue of employing wavefront features which determine whether the reticule is out of focus. Singh teaches an optical system for determining gate dimensions. By comparing signals associated with the gate to those previously stored from

various measurements, the gate dimensions can be determined. Yoshitake teaches management of an exposure process using optical scatterometry apparatus.

None of the foregoing references considered singly or in combination teach or even suggest the recited "preparation step" comprising:

> *preliminarily forming on a sample wafer a test pattern ... and an actual circuit pattern...;*
>
> .
>
> .
>
> .
>
> *calculating a first correspondence relationship between the feature of the test pattern and the feature of the actual circuit pattern, and a second correspondence relationship between the process parameter[used to make the sample wafer] and the measured features[of the test pattern and the actual circuit pattern]*

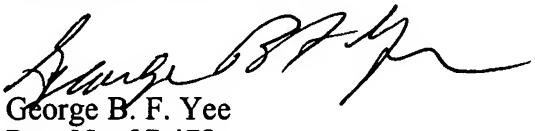
and using the first and second correspondence relations on a manufactured wafer to "evaluate the semiconductor manufacturing process line for an actual circuit pattern" on the manufactured wafer, as recited in pending claim 16.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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